IN THE CLAIMS

Please amend claims 1, 4-10, and 13-19 as indicated below.

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1. (Currently Amended) A method comprising:

enabling a special programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for program verification and wherein the enabling special programming mode disables internal program verification by the memory;

programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification; and

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exiting the special programming mode of the memory.

2. (Original) The method of claim 1, further comprising verifying the plurality of words programmed into the memory with a verification processor by resending the plurality of words previously sent into the memory.

3. (Original) The method of claim 2, wherein the verification processor is an external host processor.

4. (Currently Amended) The method of claim 2, further comprising enabling internal program verification by the memory and wherein the verification processor is ~~the memory~~ an internal program verification processor of the memory.

5. (Currently Amended) The method of claim 2, wherein the verifying further includes:

determining if all of the words in the plurality of words are verified;

if any one of the plurality of words does not verify, then ~~repeat~~ repeating the programming of the entire plurality of words and ~~repeat~~ repeating the verification; and

if all of the plurality of words verify, then exiting the special programming mode of the memory.

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6. (Currently Amended) The method of claim 2, wherein the verifying further includes:

determining if all of the words in the plurality of words are verified;

if any one of the plurality of words does not verify, then ~~repeat~~ repeating the programming of the one word that did not verify and ~~repeat~~ repeating the verification; and

if all of the plurality of words verify, then exiting the special programming mode of the memory.

7. (Currently Amended) The method of claim 1, wherein upon exiting the special programming mode of the memory, ~~permanently disables~~ the special programming user interface is permanently disabled.

8. (Currently Amended) The method of claim 1, wherein upon exiting the special programming mode of the memory, the ~~enables~~ internal program verification by the memory is enabled.

9. (Currently Amended) The method of claim 1, wherein programming of the plurality of words into the memory ~~further~~ comprises using only a single programming pulse for each bit of each word of the plurality of words.

10. (Currently Amended) The method of claim 1, wherein the programming of the plurality of words into the memory without the memory performing internal program verification continues until a programming ending condition is met.

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11. (Original) The method of claim 10, wherein the programming ending condition is a pre-selected time.

12. (Original) The method of claim 10, wherein the programming ending condition is an ending address.

13. (Currently Amended) An apparatus comprising:

a memory comprising:

an automation circuitry to perform internal program verification unless disabled;

a special programming mode circuitry to disable the internal program verification by the ~~memory~~ automation circuitry when the special programming mode circuitry is enabled; and

a host processor communicatively coupled to the memory, the host processor including:

a circuit to send to the memory a plurality of words to be programmed into the memory without the memory performing internal program verification during the special programming mode; and

a circuit to exit the special programming mode of the memory.

14. (Currently Amended) The apparatus of claim 13, wherein the host processor further includes a circuit to verify the plurality of words programmed into the memory ~~including a verification processor~~.

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15. (Currently Amended) The apparatus of claim 14, wherein the host processor includes a verification processor to verify the plurality of words programmed into the memory ~~is an external host processor~~.

16. (Currently Amended) The apparatus of claim 14, ~~further including enabling internal program verification by the memory and wherein the~~ wherein the memory further comprises a verification processor to perform internal program verification, when the special programming mode is disabled ~~is the memory internal program verification processor~~.

17. (Currently Amended) The apparatus of claim 14, wherein the circuit to verify ~~verifying further~~ includes:

circuitry to determine if all of the words in the plurality of words are verified ~~including: a second memory coupled to the host processor~~; and

circuitry to compare ~~for comparing~~ the plurality of words stored in ~~the~~ a second memory coupled to the host processor with a plurality of words read from the memory by the host processor.

18. (Currently Amended) The apparatus of claim 17, wherein the host processor further comprises ~~further including~~:

a circuit to reprogram the entire plurality of words if any one of the plurality of words does not verify.

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19. (Currently Amended) The apparatus of claim 17, wherein the host processor further comprises ~~further including~~:

a circuit to reprogram one or more words that are not verified ~~one word that did not verify~~.

20. (Original) The apparatus of claim 13, wherein the circuit to exit the special programming mode of the memory disables the special programming mode circuitry.

21. (Original) The apparatus of claim 13, wherein the circuit to exit the special programming mode of the memory enables internal program verification by the memory.

22. (Original) The apparatus of claim 13, wherein the special programming mode circuitry is disabled when a programming ending condition is met.

23. (Original) The apparatus of claim 22, wherein the programming ending condition is a pre-

selected time.

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24. (Original) The apparatus of claim 22, wherein the programming ending condition is an ending address.